WHAT IS CLAIMED IS:

1. A shared delay circuit of a semiconductor device comprising:

an input signal conversion unit for converting a plurality of input signals into a plurality of pulse signals;

a delay unit for delaying the pulse signals outputted from the input signal conversion unit for a predetermined time to output the delayed pulse signals; and

a switch and output control unit for receiving the pulse signals outputted from the input signal conversion unit and the delayed pulse signals delayed for the predetermined time through the delay unit, and outputting the delayed pulse signals in the same form as the input signals inputted to the input signal conversion unit.

2. The shared delay circuit of claim 1, wherein the input signal conversion unit has a plurality of pulse conversion units which correspond to the plurality of input signals.

3. The shared delay circuit of claim 1, wherein the input signals are level signals or pulse signals.

4. The shared delay circuit of claim 1, wherein the delay unit comprises:

a pulse signal detection unit for detecting whether one of the plurality of pulse signals is activated; and

a delay control unit for receiving and delaying an output of the pulse signal detection unit for a predetermined time, and outputting the delayed output of the pulse signal detection unit.

5. The shared delay circuit of claim 4, wherein the pulse signal detection unit comprises a NAND gate or a NOR gate.

6. The shared delay circuit of claim 1, wherein the switch and output control unit comprises a plurality of switch and output control units which correspond to the plurality of pulse signals; and

wherein the switch and output control units are activated by the pulse signals, and converts the delayed pulse signals into a form of the input signals.

7. The shared delay circuit of claim 1, wherein the switch and output control unit comprises a plurality of switch and output control units which correspond to the

plurality of pulse signals, and each of the switch and output control unit comprises a switch, a switch control unit and a control unit; and

wherein the switch control unit controls an on/off operation of the switch, the switch passes therethrough and applies the delayed pulse signal to the control unit, and the control unit converts the input delayed pulse signal into the input signal form.

8. The shared delay circuit of claim 7, wherein the switch control unit enters into a standby mode by an output signal of the control unit.

9. The shared delay circuit of claim 7, wherein after the output signal is outputted from the control unit, the switch control unit and the control unit compulsorily enter into a standby mode by an external signal.

10. A shared delay circuit of a semiconductor device receiving a plurality of input signals and delaying the plurality of input signals for a predetermined delay time using one shared delay circuit.

11. The shared delay circuit of claim 10, wherein the

circuit converts the input signals into pulse signals, delays the pulse signals for the predetermined time, and converts the pulse signal in the same form as the input signals.